System Architecture

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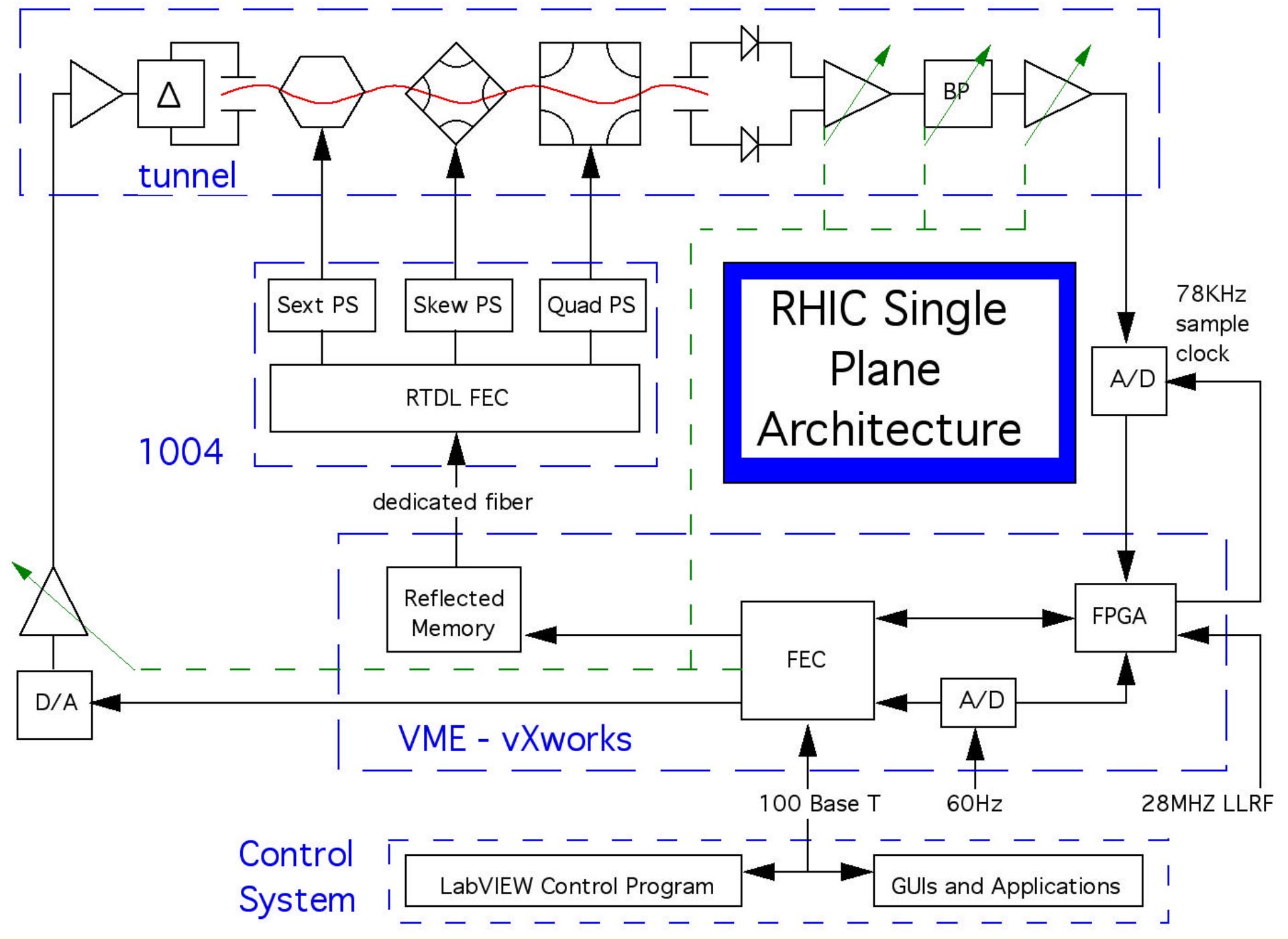
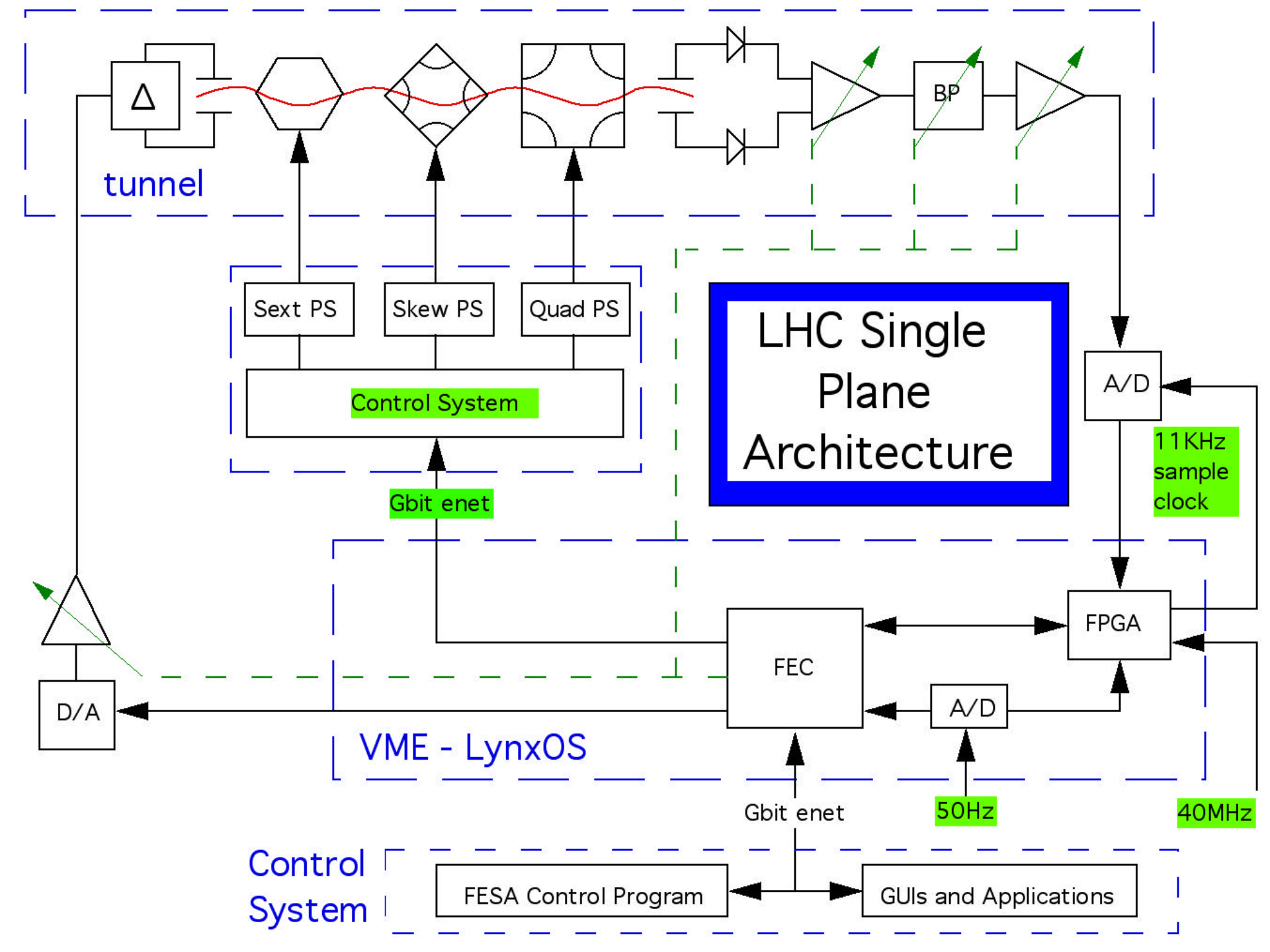
Outline

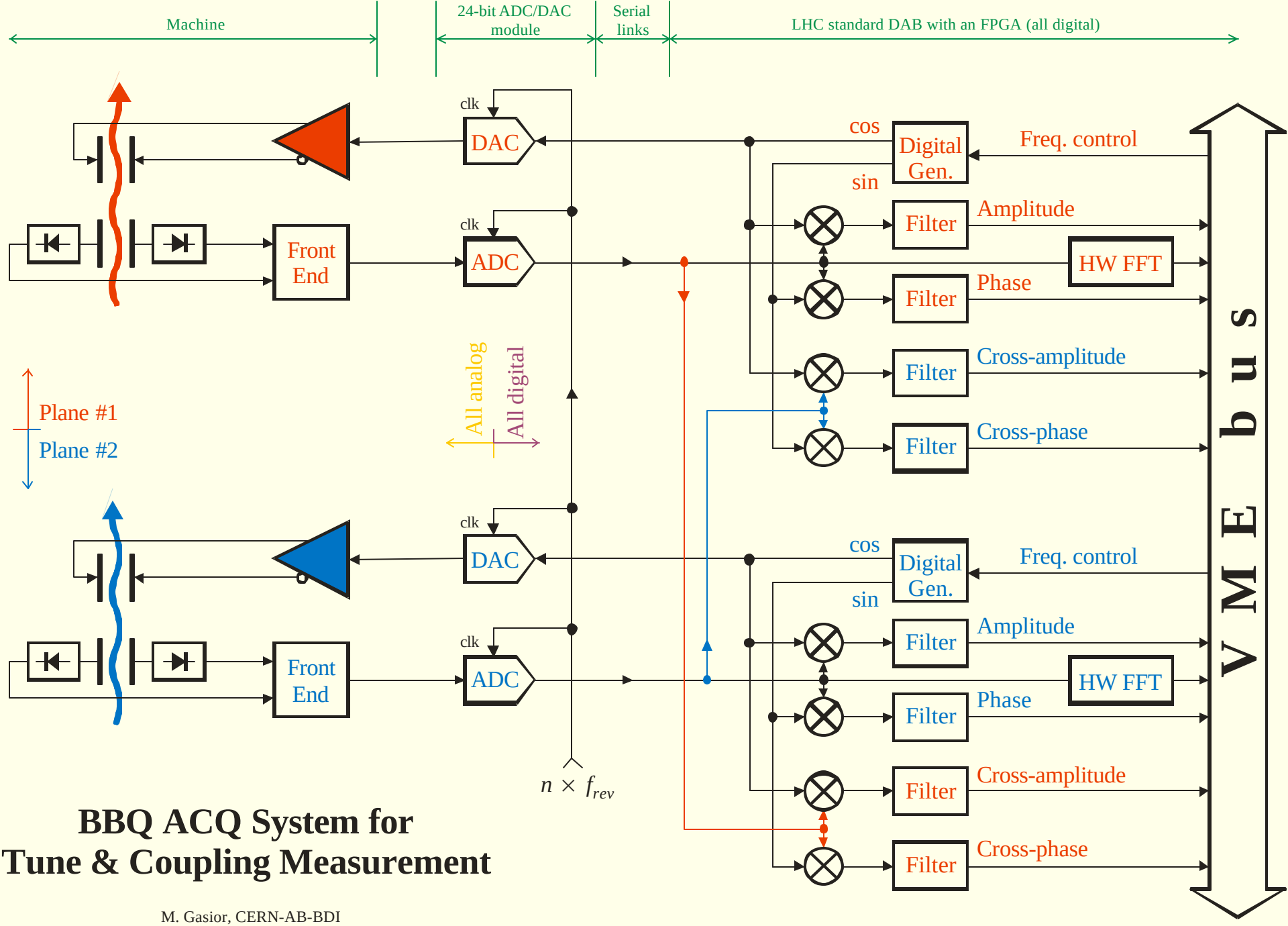
- Constraints
- The RHIC Single Plane Architecture
- The LHC Single Plane Architecture
- Two Planes and Coupling Measurement
- The Codec
- Boundaries

Constraints

- Hardware compatibility between RHIC and LHC
  - essentially the same beams, at different frequencies
- Software compatibility between RHIC and LHC
  - common platform - VME
  - vXworks (BNL) and lynxOS (CERN)
  - LabVIEW???
- Maintainability, Obsolescense,...
- Manpower - keep it simple
- Schedule

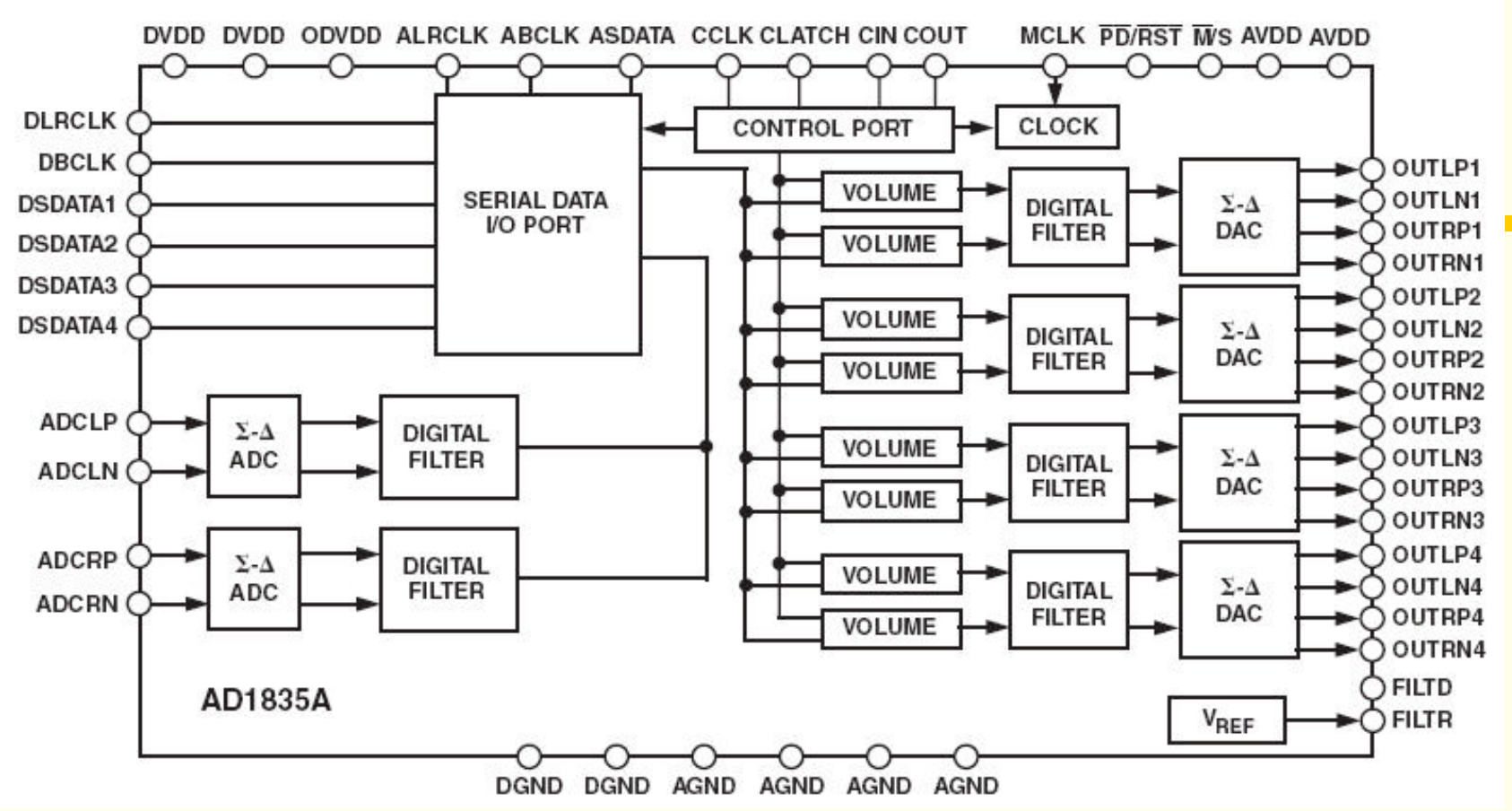

RHIC Single Plane Architecture
tunnel
BP
Sext PS
Skew PS
Quad PS
RTDL FEC
1004
dedicated fiber
78KHz sample clock
A/D
Reflected Memory
FEC
FPGA
D/A
A/D
VME - vXworks
100 Base T
60Hz
28MHZ LLRF
Control System
LabVIEW Control Program
GUIs and Applications


tunnel
Δ
BP
Sext PS
Skew PS
Quad PS
Control System
Gbit enet
LHC Single Plane Architecture
A/D
11KHz sample clock
FPGA
FEC
A/D
D/A
VME - LynxOS
Gbit enet
50Hz
40MHz
Control System
FESA Control Program
GUIs and Applications

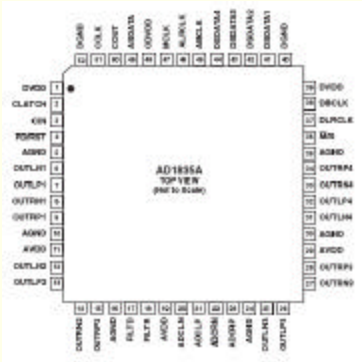


BBQ ACQ System for Tune & Coupling Measurement

M. Gasior, CERN-AB-BDI



- In one chip 2 ADCs / 8 DACs, 24 bit, 96 kS/s
- SNR 105 dB (i.e. some 18 true bits)
- It can work with any sampling frequency (< 96 kS/s)
- Everything controlled through a single bus (a few serial links)
- Some digital filters already inside



Audio Codec

Boundaries

- CERN
  - kicker amplifier, kicker, and pickup
  - Direct Diode Detection AFEs
  - Digitizer boards
  - DAB64 Boards
  - VME crate and crate computers for CERN installation
- LARP
  - VME crate and crate computers for LHC test installation at BNL
  - gate array programming
  - FEC programming
  - LabVIEW control program, collaboration on CERN equivalent
  - specification and testing of LHC TF Applications software
  - testing at RHIC, with and without beam
  - commissioning support